Antmicro DC-SCM board rework: ESPI/LPC pins, v1

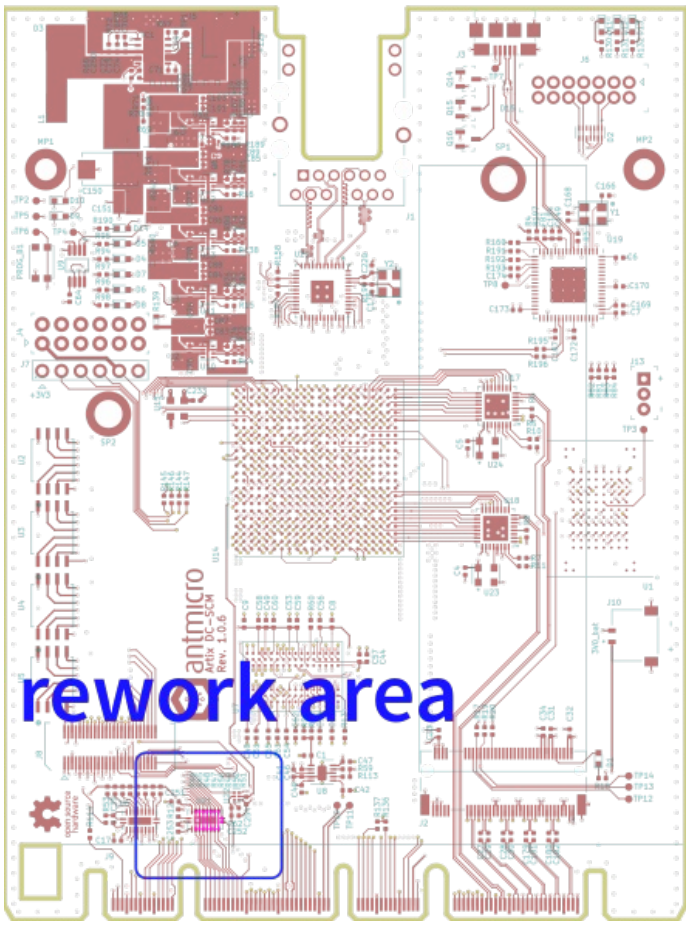
Contact: Jeremy Kerr <jk@codeconstruct.com.au>

Objective is to bypass a no-pop voltage translator, U21. Without U21 populated, the ESPI pins on the DC-SCI connector are NC. On POWER9 platforms, the LPC bus is 3.3V, so the translator is not needed, and we can connect the DC-SCI ESPI pins (used for LPC in this case) directly to the Artix FPGA.

Original board design is from Antmicro, at https://github.com/antmicro/artix-dc-scm .

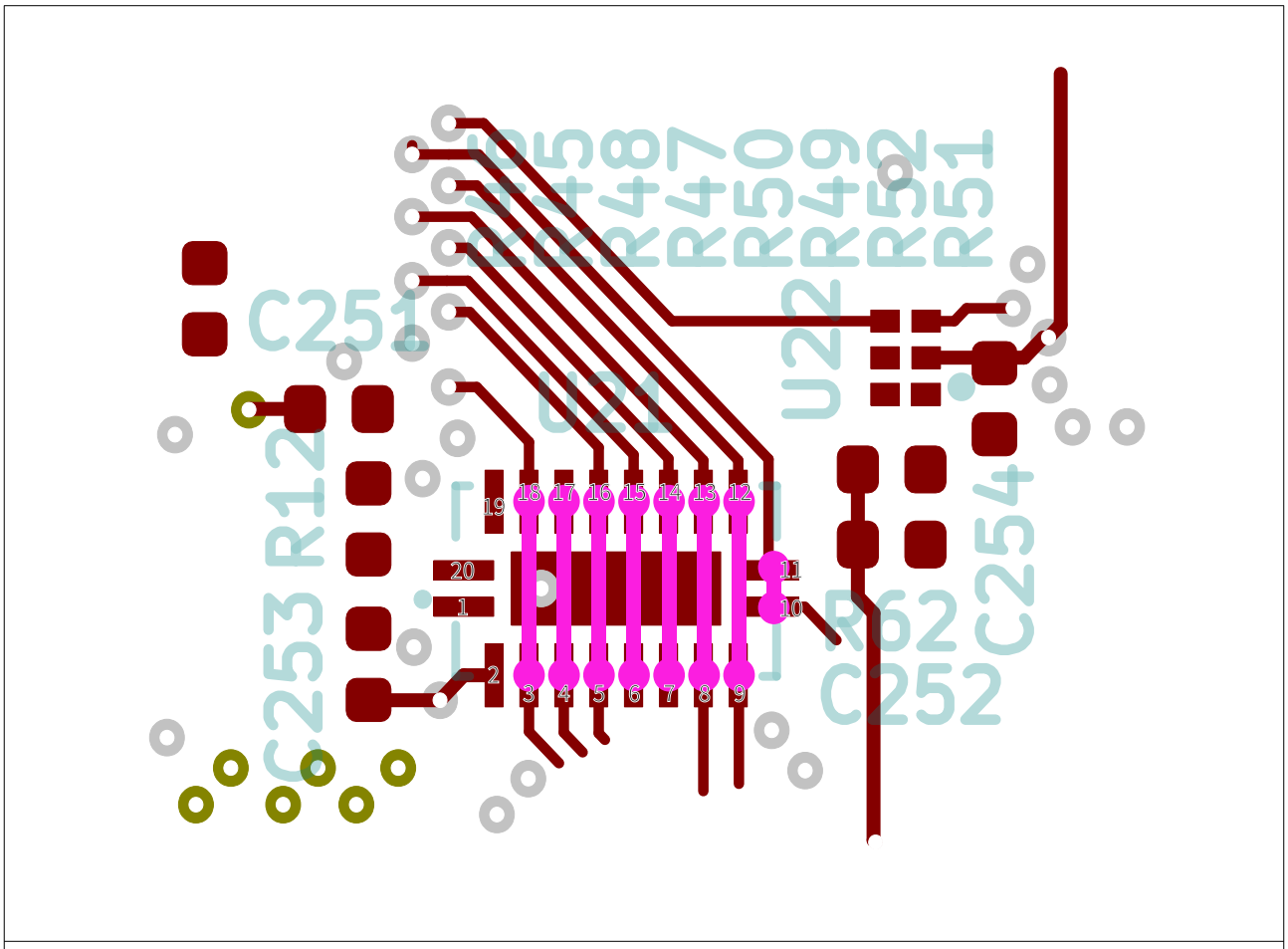
code construct

Outline



General area is towards edge-connector side of board, component U21.

Detail



New connections (marked in pink) across 8 opposing pins of (no-pop) U21:

3 —18
4 —17
5 —16
6 —15
7 —14
8 —13
9 —12
10—11 (on RHS of U21)

Connections isolated from central ground pad of footprint.

Pins 1, 2, 19 and 20 remain NC.
GND pad in center of footprint NC.